WHAT IS CLAIMED IS:

1. A power supply circuit for use with a semiconductor tester to power a device-under-test, the power supply circuit including:

power generation circuitry disposed in the tester and having an output to generate power for the device-under-test; and

load circuitry selectively coupled to the power generation circuitry output and disposed within the tester to selectively simulate the electrical loading of a device-under-test on the power supply.

2. A power supply circuit according to claim 1 wherein the load circuitry comprises calibration circuitry.

3. A power supply circuit according to claim 2 wherein the internal calibration circuitry includes:

an active DC load.

4. A power supply circuit according to claim 3 wherein the active DC load includes:

a plurality of FETs disposed in parallel to selectively cooperate and provide a variable resistance.

5. A power supply circuit according to claim 3 and further including:

a NIST-traceable current source selectively coupled to the active DC load.

6. A power supply circuit according to claim 1 and further including:

a power supply housing; and

the power generation circuitry, and the load circuitry and the switching circuitry are disposed within the power supply housing.

7. A power supply circuit according to claim 1 wherein:

the power generation circuitry comprises first and second power supply units disposed in parallel and having respective outputs, each power supply unit having respective force and sense lines coupled to the DUT; and

the load circuitry comprises first and second load circuits corresponding to the first and second power supply units and disposed respectively at the power supply unit outputs, the power supply circuit further including switching circuitry operative to selectively place the load circuitry from the second power supply unit in a closed-circuit with the first power supply unit and the force and sense lines from the first and second power supply units.

8. A power supply circuit according to claim 2 wherein the load circuitry further includes:

validation circuitry disposed within the tester and coupled to the power generation circuitry.

9. A power supply according to claim 8 wherein the internal validation circuitry includes:

AC load circuitry; and

capacitive load circuitry.

10. A power supply circuit according to claim 1 wherein the internal load circuitry comprises internal validation circuitry.

11. A power supply circuit according to claim 10 wherein the internal validation circuitry includes:

AC load circuitry; and

capacitive load circuitry.

12. A power supply circuit according to claim 10 and further including:

internal calibration circuitry disposed within the tester and coupled to the power generation circuitry.

13. A power supply according to claim 12 wherein the internal calibration circuitry includes:

an active DC load.

14. Automatic test equipment for testing a device-under-test, said device-under-test disposed on a device board, the automatic test equipment including:

a computer workstation;

a testhead coupled to the computer workstation; and

a device-under-test power supply, the device-under-test power supply including

power generation circuitry disposed within the testhead to generate power for the device-under-test; and

load circuitry disposed within the testhead and coupled to the power generation circuitry, the load circuitry operative to selectively simulate the electrical loading of a device-under-test on the power supply.

15. A method of calibrating an ATE power supply current measurement unit without undocking a semiconductor tester from a device handling apparatus, the device handling apparatus mounting a device-under-test, the ATE power supply current measurement unit being initially coupled to the device-under-test, the method including the steps of:

selecting an in-tester load having a known impedance;

substituting the device-under-test with the in-tester load, such that the ATE power supply current measurement unit is coupled to the in-tester load;

measuring a first current with the current measurement unit;

determining a second current by detecting the voltage across the in-tester load, and dividing the voltage value by the known impedance;

comparing the first current to the second current to calculate an offset current; and

assigning calibration values to compensate for the calculated offset current.

16. A method of validating a DUT power supply without undocking a semiconductor tester from a device handling apparatus, the device handling apparatus mounting a device-under-test (DUT), the DUT power supply being initially coupled to the DUT, the method including the steps of:

selecting a dynamic in-tester load having variable dynamic load characteristics;

substituting the device-under-test with the in-tester load, such that the DUT power supply is coupled to the in-tester load;

driving the dynamic in-tester load with the DUT power supply; and

confirming that the DUT power supply operated within predetermined performance parameters during the driving step.

17. A method of validating a DUT power supply without undocking a semiconductor tester from a device handling apparatus, the DUT power supply comprising first and second power supply units disposed in parallel, each power supply unit being switchably coupled to the DUT via respective force and sense lines, and each unit having respective first and second in-tester dynamic loads, the method including the steps of:

selecting the first power supply unit for coupling with the DUT;

substituting the in-tester load associated with the second power suplly unit for the DUT;

driving the second in-tester load through the respective force and sense lines with the first power supply unit; and

confirming that the first power supply unit operated within predetermined performance parameters during the driving step.